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The LEDA512 integrated circuit anode array for the analog recording of mass spectra

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Abstract

This article describes two generations of a novel integrated circuit multi-anode electron detector chip (LEDA512). This chip is designed for usage as an analog ion detector in magnetic mass spectrometers, in combination with a stack of two micro channel plates. The first generation chip is applied in a positive ion mass spectrometer on-board the ESA ROSETTA cometary mission. The detector chip comprises two identical and redundant parts, each consisting in a row of 512 rectangular anodes for electron collection, and in an anode multiplexer followed by a charge amplifier. A second-generation of the chip is scheduled. It will implement additional features, such as: radiation hard MOS transistors and shift registers and improved output drive capabilities. (Int J Mass Spectrom 215 (2002) 77–87) © 2002 Elsevier Science B.V. All rights reserved.

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1. Introduction

Mass spectrometers exist in many different configurations. Some of these, in particular the double focussing magnetic mass spectrometer type, have detector systems capable of simultaneously detecting different ion species in their focal plane. They are therefore, equipped with a focal plane array consisting of a stack of two or three micro channel plates (MCPs)—for efficient, high gain conversion of the ion charge to a charge cloud composed of electrons—combined with either a phosphor-based electron-to-photon conversion system and photodiode arrays, or with some kind of multi-anode device. The detector system can then either be digital (event oriented) or analogue (accumulated charge oriented).

In this paper, we focus on a specific multi-anode device that is in the first place analogue and in the second place fully integrated. The need for such a device appeared during the design phase of the double focussing mass spectrometer (DFMS), part of the Rosetta Orbiter Spectrometer for Ion and Neutral Analysis (ROSINA) [1], an instrument that will be on-board the ESA ROSETTA spacecraft. ROSETTA [2] is a planetary corner stone mission of the European Space Agency scheduled for launch in 2003 and for an encounter with comet 46 P/Wirtanen in 2011.

The main reason why an analogue multi-anode detector was selected was that for this mission a large sensitivity range of 10 orders of magnitude was

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desired, in combination with the ability for simultaneous detection of a series of mass peaks. This large sensitivity range can be obtained as the product of more than six orders of magnitude for the MCP gain range, in combination with almost four orders of magnitude dynamic range for the detector system. This would not have been feasible with an event driven detector system.

The collection of the MCP output charge cloud with high spatial resolution, low noise and the desired dynamic range is possible by means of the linear electron detector array chip with 512 anodes (LEDA512), described hereafter. The chip integrates two identical, but totally independent detector units. Each unit is composed of a row of 512 separate floating anodes, an analog multiplexer addressed by a digital shift register, an on-chip voltage reference and a charge sensitive amplifier.

In the following sections, the architecture and operation of the first generation version of the detector chip, which has already been described in detail elsewhere, will be presented. Furthermore, details will be shown about the improvements that have led to the second generation of the LEDA512, which is now being manufactured (LEDA512-V2). The design, operation and testing of the complete detector system for the ROSINA DFMS mass spectrometer, which consists of three different detectors (a channeltron-slit combination, a Faraday cup-slit combination and this multi-anode array) will be handled in a companion paper [3].

2. The first generation LEDA512 anode array

2.1. Detector system concept

As explained before the LEDA512 chip's first application is for the measurement of ion spectra in a double focussing ion mass spectrometer (ROSINA DFMS). Ions are selected by the mass spectrometer according to their mass-to-charge ratio and impact at different places on a focal plane detector. The front side of a stack composed of two MCP devices is positioned in this focal plane and the LEDA512 chip itself is mounted in close proximity of the MCP stack's back. Each time an ion impacts on the front side of the MCP, the latter ejects a packet containing $1 \approx 10^6$ electrons/ion, depending upon the MCP supply voltage setting, the impacting ion type and the ion energy. The electrical field applied between the stack's back face and the anode array chip guides the electrons, produced by the MCP, towards the floating anodes of the chip's anode array. The width of a single anode was fixed at 25 μm, a value matched with the predicted mass resolution of the DFMS mass spectrometer. A mathematical model, predicting the spatial spreading of the electron packets exiting the MCP stack as a function of the applied field and of the energy of the electrons exiting from the MCP stack, was devised by our colleagues of IPSL-CETP (St. Maur-les-Fossées, France). They also designed and constructed the MCP part of the detector system, as well as the flange on which it was mounted. The number of anodes has been limited to 512 because of chip size limitations imposed by chip manufacturing. The height of the anodes (direction parallel to the spectral lines and perpendicular to the anode row) is 16 mm, a value compatible with the total height of the spectral lines of the DFMS mass spectrometer. Each anode was further split in two equal parts having a height of 8 mm, so that finally two identical rows of 512 anodes, each having an area of 25 μm × 8 mm or 0.2 mm^2, were obtained.

2.2. General chip architecture

Since the ROSINA instrument will be flying on a long duration space mission, it is important to have a reliable detector system. Therefore, from the very beginning of the anode array design, it was considered that redundancy was needed to avoid a single point of failure in the detector. An obvious way of implementing redundancy on the chip level was to integrate on the same chip two identical, but independent, arrays with matched characteristics, each possessing its own independent power supply, clock and output lines. The layout of both anode arrays and their

associated on-chip electronics is mirrored with respect to the central axis of the chip.

Because the two redundant chip halves are identical we need only to present the block diagram of half of it (see Fig. 1). One such integrated unit consists of the anode array itself, the anode selection switches for anode read-out and recharge, the digital logic to command the switches in the right order, an internal reference circuit, the charge amplifier (CSA) and the CSA reset circuitry. In addition, output buffers bring the CSA output and the reference voltage off-chip.

Fig. 2 shows, a photograph of the complete chip as mounted on a custom designed ceramic support that is compatible with the DFMS mounting and wiring rules. One recognizes the chip, the ceramic, the bonding wire area and the connector pin area.

2.3. Anode array read-out

Each of the two redundant anode arrays is read-out serially, i.e. anodes are read-out one after another. This is accomplished at a nominal clock speed of 100 kHz (10 μs period) by means of only three digital control lines *clock*, *start* and *reset*. During a read-out cycle each anode is selected in sequence, connected to the charge amplifier input and precharged to the internal chip reference level V_{ref} (≈2.3 V). Q_{signal}, the charge associated with the signal output of the MCP, is integrated on each floating anode between two consecutive read-out cycles and hence between consecutive anode precharges. This charge is transferred to the feedback capacitor C_{f} of the CSA while the specific anode is connected to the CSA input, which is virtually at the internal reference potential. As a result of the read-out cycle the differential output $(V_{\mathrm{out}} - V_{\mathrm{ref}})$ of the CSA will be a train of analog pulses having amplitudes equal to 0 when there is no signal and to

$$V_{\mathrm{out}} - V_{\mathrm{ref}} = \frac{Q_{\mathrm{signal}}}{C_{\mathrm{f}}} \tag{1}$$

when signal charge is being integrated on the anodes. The effective output signal is the difference between V_{out} and V_{ref}, which are both available as outputs. The inevitable process induced variations on the anode capacitance and amplifier gain do not lead to charge-to-voltage conversion non-uniformity, since there is only one charge amplifier and one feedback capacitance for all anodes.

The anode capacitance and the allowable anode voltage range determine how much charge may be collected between anode recharges. The anode capacitance is completely determined by the size of the anode metal (25 μm × 8 mm) and by the characteristics of the dielectric layer used in the chip. The 0.7 μm CMOS process (Alcatel Microelectronics), used to manufacture the chip, results in an anode capacitance of 4.22 pF. If we allow the anode voltage at maximum to decrease 2 V below V_{ref} while electrons from the MCP are being collected, this corresponds to a maximum integrated negative anode charge of 8.44 pC per read-out.

2.4. Anode array protection against excess charge

Protection of anodes against excess charge is an important issue and therefore each individual anode needs its own protection circuit. Several causes for unwanted anode charge built-up may exist: charge created during chip manipulation, leakage currents to or from parts in the neighborhood of the detector and finally charge built-up during long periods without detector read-out or when the detector is over-exposed.

Concerning the latter situation one might think that, since negative charges (electrons) coming from the MCP are collected and lower the anode voltage, the anode potential can never rise above the recharge voltage V_{ref}. However, the inverse situation may exist if the field between the MCP back side and the LEDA512 chip is reversed so that secondary electrons, created when electrons impact on an anode, are favored to escape from the anode surface. In the latter case, the anode voltage may rise with signal, beyond V_{ref} and eventually beyond the chip's supply voltage. A reverse biased, low leakage clamping diode is inserted between each anode and the positive supply to protect against this situation. The situation with the reversed field may be voluntarily created to operate

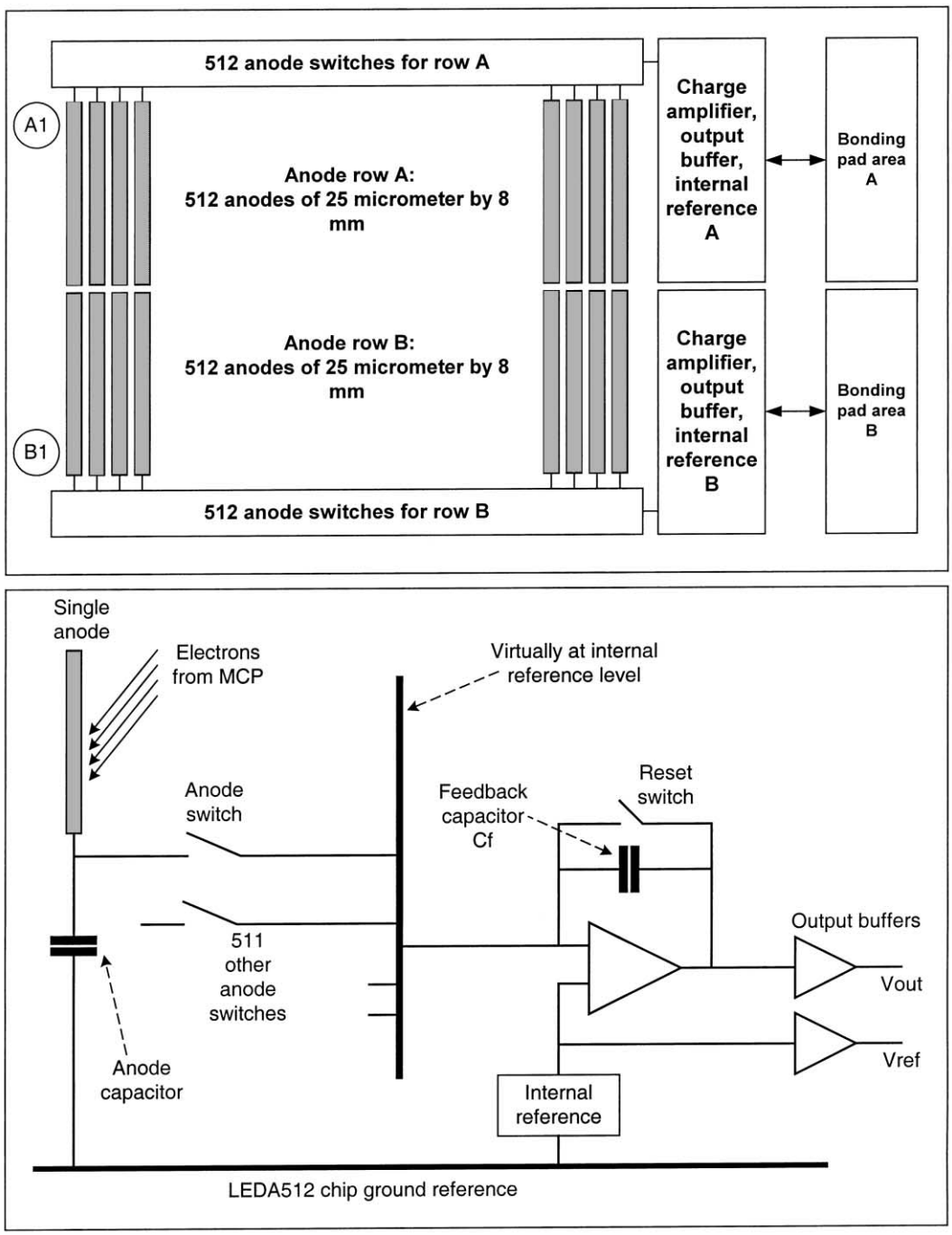

Fig. 1. Block diagram. Upper part: lay-out of the different parts of the LEDA512 chip; lower part: internal organization of one of two identical, redundant chip halves.

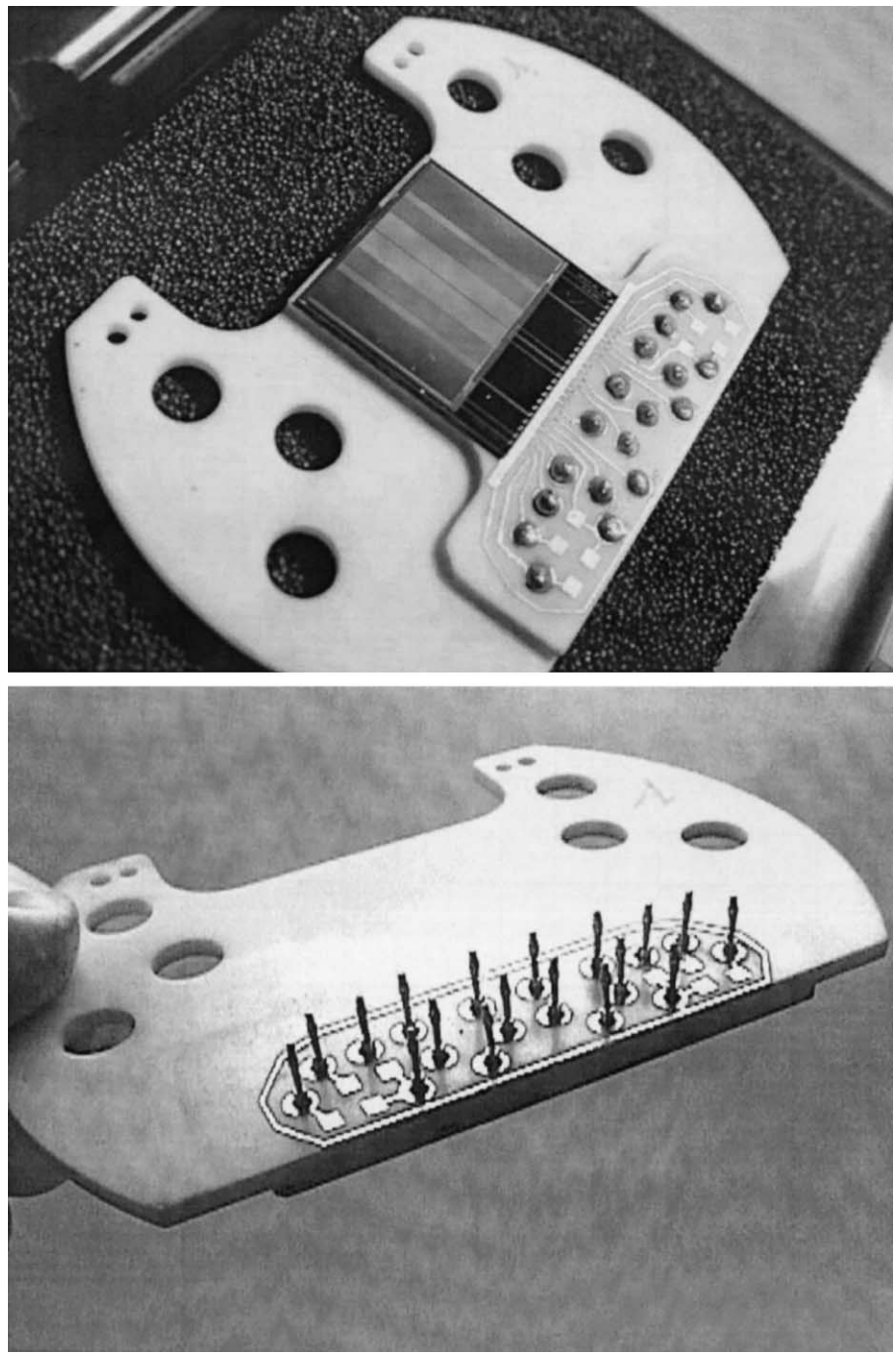

Fig. 2. Photograph of the LEDA512-V1 anode array chip mounted on a custom designed ceramic support. Upper part: anode side; lower part: backside of the ceramic support.

the MCP-LEDA512 assembly in a special mode (see companion paper [3]).

The protection circuits also include a voltage clamp circuit that monitors the voltage difference between each anode and the chip's ground reference. As long as the voltage level on the anode remains at least 300 mV above ground, this circuit remains non-conducting. If the anode is further discharged, due to for example a very intensive mass peak, positive charge is injected into the anode, which compensates for the excess negative charge input. This solution is preferred rather than a simple diode clamp connected to ground, because a diode would inject excess charge into the chip's substrate, thus, provoking leakage effects in neighboring structures. The influence of the complete protection circuit on the anode leakage current is minor. The impact on the anode capacitance may be disregarded as well, since the protection circuit introduces an extra capacitance of only 5 fF per anode.

2.5. Anode selection switches and charge amplifier

Each of the 512 floating anodes is connected during a short period of time to the charge amplifier input for charge transfer and precharge. This connection is accomplished by means of one out of 512 anode selection switches, forming a 512-to-1 multiplexer controlled by a digital shift register, which itself is driven by the *clock* and *start* signals. A common bus line connects the selected anode with the inverting input of the CSA, which has a feedback capacitance of 6 pF. The charge amplifier output and the reference voltage, which are both needed for the differential read-out of the anode signal, are buffered by two unity gain buffers.

2.6. Special geometric and electric precautions

The bonding pads (input, output and supply connection areas) on the LEDA512 anode array are positioned on a line along its border at a safe distance (5 mm) between the pads and the active area where the charge collection is performed. This is necessary in order to avoid contact between bonding wires and the back side of the MCPs. Additionally, a metal shielding layer forms a conductive ring around the anode area. It has a width of 400 μm on the bonding side and of 600 μm on the three other sides. A separate bonding pad is connected to this ring allowing for independent external control of its voltage setting.

2.7. Noise and baseline performances

The baseline of the integrated anode array read-out is well under control. Two effects play a role: noise and influence of leakage current.

The differential voltage appearing at the output of the LEDA512 chip is handled by a 12-bit analog-to-digital converter (ADC) system, which is part of the ROSINA DFMS space borne electronics. The maximum voltage swing allowed on the anodes implies that a maximum charge of 8.44 pC can be integrated without saturation effects. The quantization noise of the ADC, 1 least significant bit (LSB), is therefore, equal to roughly 13,000 e^- rms. As was shown in a previous paper [4] the total noise of the LEDA chip itself (reset noise, amplifier noise, etc.) is at most 0.1 LSB and hence there is no need for more complicated readout schemes that suppress noise, as for example correlated double sampling.

Fig. 3 demonstrates, besides other effects, the real noise result obtained by the combination of the LEDA512 and its read-out electronics. As is demonstrated by the accumulation of many similar read-outs of a LEDA512 chip mounted on the DFMS detector flange (no voltage on the MCP), no systematic noise features appear (less than 0.1 LSB per read-out), even no systematic noise originating from the ADC, digital clocks or supply lines. For a single read-out the noise is within ±0.5 LSB, as one would expect for such a system.

The influence of charge leakage to the read-out baseline can be demonstrated in two ways. Fig. 4 shows the effect of long charge integration times on the anode array read-out baseline. There is an observable effect related to integration time: in the extreme case of a charge integration during 6.55 s, it amounts to

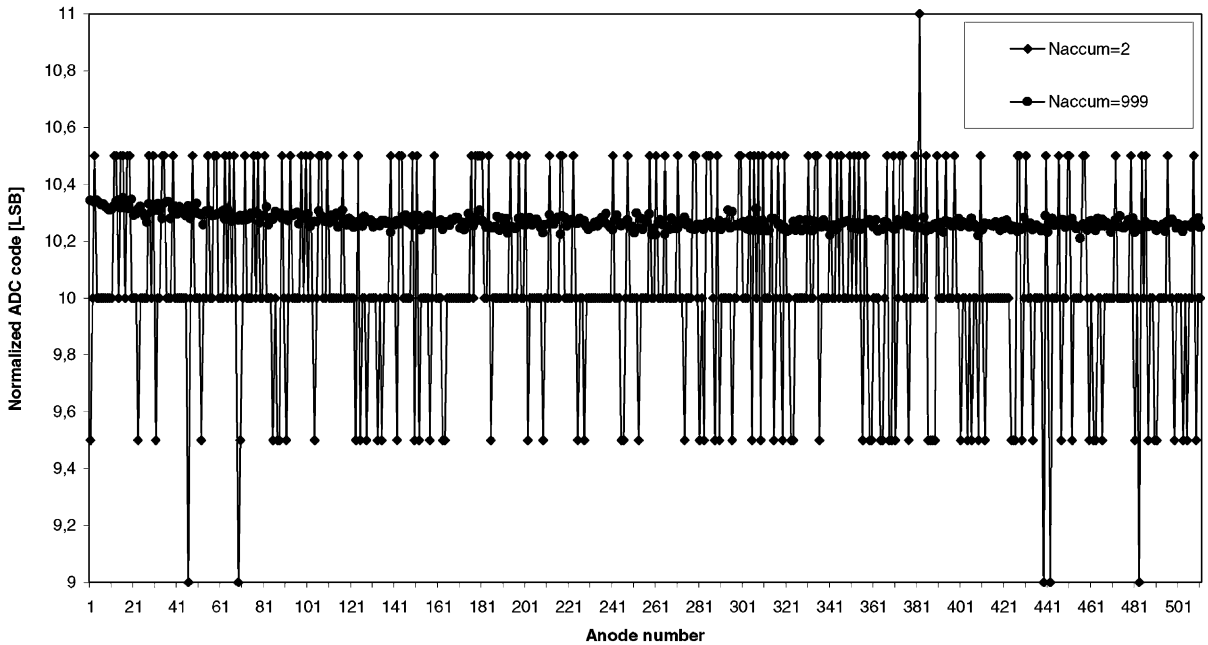

Fig. 3. Real noise performance obtained from the LEDA512 + read-out electronics (MCP high-voltage supply disabled) by spectrum accumulation. Two cases are shown: 2 and 999 accumulations.

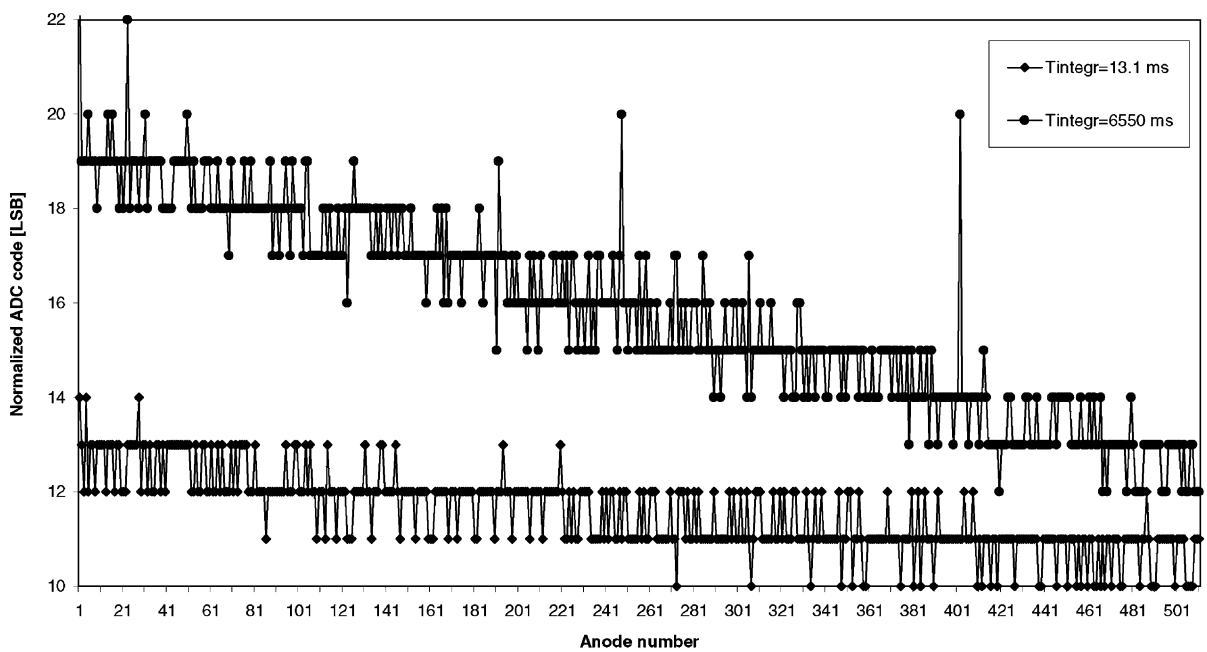

Fig. 4. Effect of long charge integration times on the anode array read-out baseline. Upper plot: integration time of 6550 ms; lower plot: integration time of 13.1 ms.

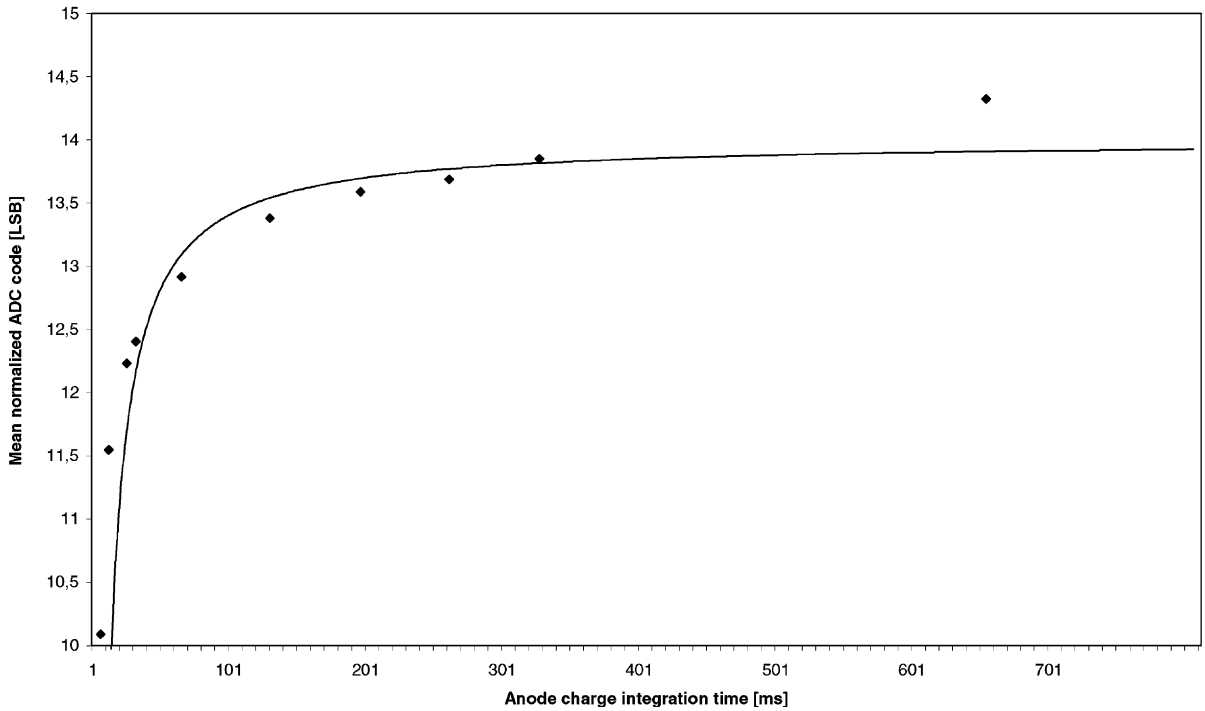

Fig. 5. Mean value over all anodes of a single array read-out (normalized to one integration time unit) as a function of integration time (◆) and corresponding simple charge leakage model (plain line).

about 6 ADC LSB per integration time unit (6.55 ms) for the first anodes and lowers to about 2 ADC LSB for the last ones. Since the LEDA512 will never be operated at very long integration times, except for performance verification, there is absolutely no problem with leakage: the latter contributes to the baseline for less than 0.1% of ADC full-scale, which may be easily subtracted from a recorded spectrum and poses no problem for the available dynamic range.

Another way to look at the influence of integration time on the baseline is to study the mean value over all anodes of a single array read-out (normalized to one integration time unit) as a function of integration time. Fig. 5 depicts these results and one can see that there are probably two effects at work on the integrated anode charge Q_{anode}. As formulated by (2) there is a current leakage effect proportional with the duration of the integration, plus a fixed charge injection effect that appears during every read-out, adds to the read-out offset and is independent of integration time.

$$Q_{\text{anode}} = Q_{\text{injected}} + i_{\text{leak}} T_{\text{integration}}. \tag{2}$$

If one now introduces the linear relationship between ADC code and anode charge

$$\text{ADC code} = aQ_{\text{anode}} + b. \tag{3}$$

One gets from (2) and (3) an expression for the normalized ADC code corresponding to both effects:

$$\frac{\text{ADC code}}{T_{\text{integration}}} = \frac{aQ_{\text{injected}} + b}{T_{\text{integration}}} + ai_{\text{leak}} \tag{4}$$

or

$$\frac{\text{ADC code}}{T_{\text{integration}}} = ai_{\text{leak}} - \frac{c}{T_{\text{integration}}} \quad \text{with}$$
$$-c = aQ_{\text{injected}} + b. \tag{5}$$

The model curve added to Fig. 5 is the combination of the two effects as expressed by (5) with the following

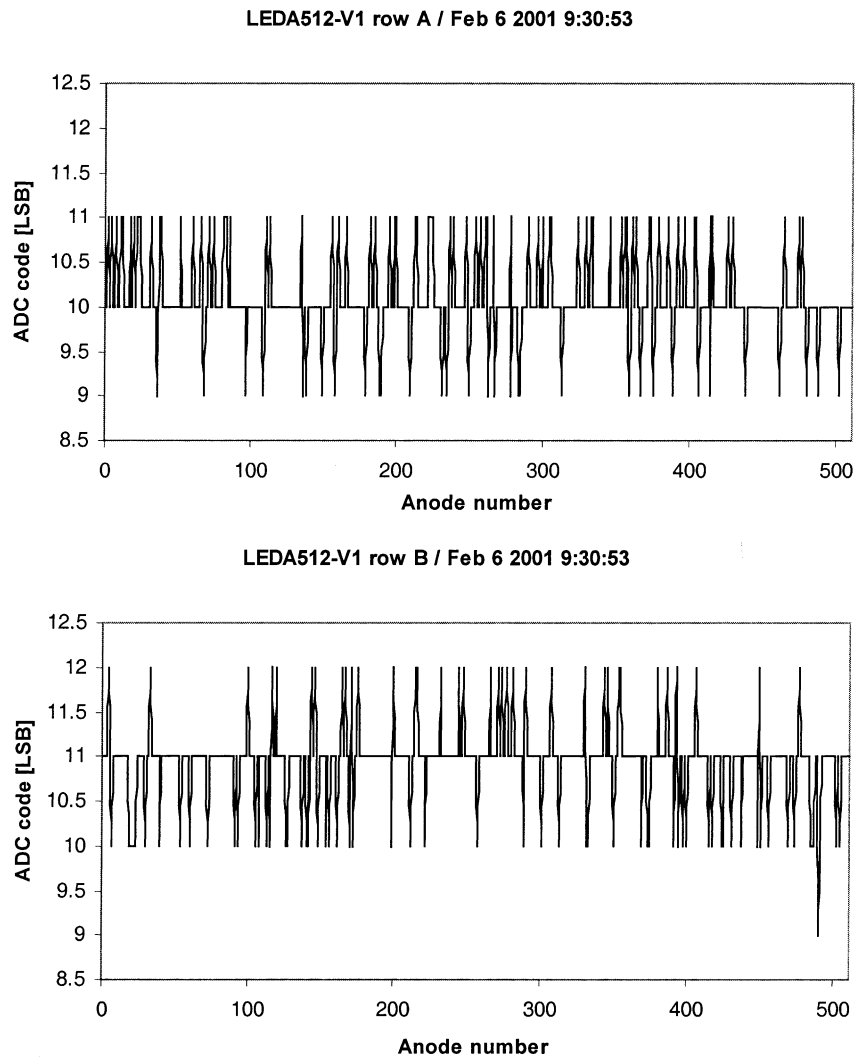

Fig. 6. Demonstration of baseline and offset differences of the detector chip parts A and B (the two separate anode arrays on the chip).

parameter choices: $ai_{\text{leak}} = 14$ ADC code LSB's per integration time unit and $c = 60$ ADC code LSB's. The rather good fit between the model and the observations tends to confirm that leakage is most probably linearly dependent on integration time and that charge injection can be compensated for by ADC offset adjustment.

From Fig. 6, one remarks further that the baselines of the detector chip parts A and B (the two separate anode arrays on the chip) show slightly different offsets. This difference is inherent to the applied amplifier/buffer configuration and to the CMOS technology used to manufacture the chip. In the case of Fig. 6, it accounts to about 1 LSB, but not one chip was found with an offset difference of more than a few percent of full scale, including the ADC offset. It can be easily corrected for by subtraction of an appropriate fixed ADC code. A second effect is the slightly different slope of both baselines, which can only be seen after many read-out accumulations. This is explained

by small differences in charge injection effects and to slightly different leakage currents in both parts.

It was also observed that after long exposures (minutes) to MCP electrons (signal) without any read-out, the detector chip baseline shows memory effects. Probably electrons from the MCP get stuck on the insulated parts of the chip surface. A few "scrubbing" read-outs, executed before normal operation of the chip, seem to remedy this problem.

2.8. Applicability

The LEDA512 anode array chip has been mounted on several laboratory set-ups and models of the ROSINA DFMS space borne mass spectrometer (Engineering, Qualification and Flight Model) with great operational success. The chip is immune to numerous power-ON/OFF cycles and to human produced static electricity. The only cause of malfunction so far has been external: a high-voltage breakdown in the MCP mounted in proximity of the chip.

Numerous spectra have been recorded by the LEDA512-MCP detector combination. The quality of the obtained spectra depends a lot on the characteristics of the complete detector and its modes of operation, both described in a companion paper [4], as well as on the resolution settings of the DFMS spectrometer. Therefore, this matter is not documented here.

3. An improved LEDA512 version 2

3.1. Ways for improvement

Although the current version of the anode array chip (LEDA512-V1) performs very well, an improved, but format and connection compatible, version was envisaged, the LEDA512-V2. It was felt that, in view of the potential application in other space projects than the ESA ROSETTA mission, the tolerance to the total dose of ionizing radiation and to single event upsets (SEUs) should be improved.

Another candidate for improvement was the driving capacity of the buffer circuits for V_{out} and V_{ref}. The present version of the chip requires an external low capacitance, high impedance voltage follower circuit, since the on-chip buffers have problems driving directly impedances lower than a few 100 kΩ.

3.2. Improvements in radiation total dose hardness

The 0.7 μm Alcatel Microelectronics CMOS process, used to manufacture the LEDA512-V1, has already a reasonable radiation dose tolerance by itself. By introducing rad hard design cells, borrowed from IMEC's space borne optical and particle detector array designs, the behavior of the circuit with respect to radiation may be improved considerably.

By an improved layout the anode switches, implemented by means of N-MOS transistors, can be hardened by at least a factor of 10^3 in terms of leakage current tolerance to total ionizing radiation dose. The same applies for the reset switch for the charge amplifier. The switch transistors in the LEDA512-V2 will get a closed design (channel surrounding the N-MOS transistor's source), as well as a guard ring around each of them that protects them against leakage currents originating from the SiO_2^-–Si interface around the transistors.

SEUs have an effect on one or more of the 512 bistable cells (flip-flops) of the digital shift register driving the anode selection switches and hence may disturb a single read-out of the chip. Here, improvement can be easily realized without changes to transistor layout. It is sufficient to replace every bistable cell by three flip-flops and majority logic. In this case a single disturbed flip-flop per cell is acceptable. The CMOS production process is known also to be intrinsically robust for latch-up.

3.3. Other improvements

The output buffers for V_{out} and V_{ref} will be improved as well. A new patented buffer layout has been designed, which is able to deliver the output voltages to 10 kΩ/100 pF loads without influencing the time response characteristics of the chip. The new design is currently being tested for radiation tolerance.

Furthermore, the CMOS process will be tuned to reduce inter-anode and anode-to-shield gaps and hence the insulation surface exposed to electrons coming from the MCP. Finally, an attempt will be made to reduce the number of driving signals required (*clock*, *start*, *reset*) by deriving *start* and *reset* on-chip from *clock*, so that simpler read-out circuits may be devised.

4. Summary and conclusions

Two generations of this linear anode array, consisting of two rows of 512 anodes, have been described.

The first generation, LEDA512-V1, has been applied in the focal plane detector of the ROSINA DFMS spectrometer, which will be launched on board of the ESA ROSETTA spacecraft in 2003. The noise and baseline performances of the detector chip in a configuration without voltages applied to the micro channel plate section of the detector, have been demonstrated by real recordings of array read-outs.

A second-generation chip, LEDA512-V2, has been described in terms of improvements with respect to its radiation tolerance, its output drive capabilities and its simplified digital control.

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